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# GUJARAT TECHNOLOGICAL UNIVERSITY DIPLOMA ENGINEERING - SEMESTER - III • EXAMINATION - SUMMER 16 

Subject Code: 3331703
Date: 17.05.2016
Subject Name: Digital Techniques
Time: 02:30 PM TO 05:00 PM
Total Marks: 70

## Instructions:

1. Attempt all questions.
2. Make Suitable assumptions wherever necessary.
3. Figures to the right indicate full marks.
4. Use of programmable \& Communication aids are strictly prohibited.
5. Use of only simple calculator is permitted in Mathematics.
6. English version is authentic.
Q. 1 Answer any seven out of ten.
7. How is a $J$ - $K$ flip-flop made to toggle?
A. $\quad J=0, K=0$
B. $J=1, K=0$
C. $\quad J=0, K=1$
D. $\quad J=1, K=1$
8. Each "1" entry in a K-map square represents:
A. a HIGH for each input truth table condition that produces a HIGH output.
B. a HIGH output on the truth table for all LOW input combinations.
C. a LOW output for all possible HIGH input conditions.
D. a DON'T CARE condition for all possible input truth table combinations.
9. A decoder can be used as a demultiplexer by $\qquad$ .
A. tying all enable pins LOW
B. tying all data-select lines LOW
C. tying all data-select lines HIGH
D. using the input lines for data selection and an enable line for data input
10. Convert binary 111111110010 to hexadecimal.
A. $E E 2_{16}$
B. $\mathrm{FF}_{1}{ }_{16}$
C. $2 \mathrm{FE}_{16}$
D. $\mathrm{FD} 2_{16}$
11. Determine odd parity for each of the following data words:
$1011101 \quad 11110111$
A. $P=1, P=1$
B. $P=0, P=0$
C. $P=1, P=1$
D. $P=0, P=0$
12. Asynchronous counters are often called $\qquad$ counters.
A. toggle
B. ripple
C. binary
D. flip-flop
13. A logic circuit that provides a HIGH output for both inputs HIGH or both inputs LOW is a(n):
A. Ex-NOR gate
B. OR gate
C. Ex-OR gate
D. NAND gate
14. Which type of gate can be used to add two bits?
A. Ex-OR
B. Ex-NOR
C. Ex-NAND
D. NOR
15. How many flip-flops are required to construct a decade counter?
A. 10
B. 8
C. 5
D. 4
16. The symbols on this flip-flop device indicate $\qquad$ .

A.triggering takes place on the negative-going edge of the CLK pulse
B.triggering takes place on the positive-going edge of the CLK pulse
C.triggering can take place anytime during the HIGH level of the CLK waveform
D.triggering can take place anytime during the LOW level of the CLK waveform
Q. 2 (a) Perform subtraction using 1's-complement method
$(10010)_{2}-(11000)_{2}$

## OR

(a) Simplify $\mathrm{Y}=\mathrm{AB}^{\prime} \mathrm{C}+\mathrm{ABC}+\mathrm{AC}^{\prime}$ using Boolean algebra.
(b) Perform subtraction using 2 's-complement method

$$
(11001)_{2}-(11000)_{2}
$$

## OR

(b) Multiply the following binary number: (101101) ${ }_{2} \mathrm{X}(101)_{2}$
(c) Two 4-bit binary numbers (1011 and 1111) are applied to a 4-bit parallel adder. The carry input is 1 . What are the values for the sum and carry output?

OR
(c) Explain the function of NAND gate as universal gate. $\mathbf{0 4}$
(d) Implement Half Subtractor circuit. 04

OR
(d) What are the differences between combinational logic and sequential logic?

OR
(a) A 4-bit up/down binary counter is in the DOWN mode and in the 1100 state. $\mathbf{0 3}$ To what state does the counter go on the next clock pulse?
(b) Implement Half Adder circuit.

## OR

(b) State De-morgan's theorems and write their expressions.
(c) How can you convert the JK Flip-flop to a D Flip-flop?

OR
(c) Draw any logic components for level loop for level switch configuration HL.
(d) Obtain SOP simplification form of following expression using Karnaugh map

$$
\mathrm{F}(\mathrm{~A}, \mathrm{~B}, \mathrm{C}, \mathrm{D})=\Sigma \mathrm{m}(1,3,4,6,9,11,12,14)
$$

OR
(d) Explain working of level loop for level switch configuration HL.
(b) Draw any logic components for temperature loop for temperature switchconfiguration LL.
(b) List applications of A/D Convertor in instrumentation. ..... 04
(c) What is a multiplexer? Implement 4:1 line multiplexer with truth-table. ..... 07
Q. 5 (a) Draw any logic components for pressure loop for pressure switch ..... 04configuration HL.
(b) Implement Full Adder circuit. ..... 04
(c) Implement Even-Parity Generator circuit. ..... 03
(d) Simplify $\mathrm{AB}^{\prime} \mathrm{C}+\mathrm{ABC}+\mathrm{AC}+\mathrm{A}^{\prime} \mathrm{B}^{\prime} \mathrm{C}$ and draw its logic diagram with ..... 03minimum gates.

