Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

DIPLOMA ENGINEERING – SEMESTER – III • EXAMINATION – WINTER- 2016

Subject Code: 3331703 Date: 22-11-2016

Subject Name: Digital Techniques

Time: 10:30 am to 01:00 pm Total Marks: 70

Instructions:

1. **Attempt all questions.**
2. **Make Suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**
4. **Use of programmable & Communication aids are strictly prohibited.**
5. **Use of only simple calculator is permitted in Mathematics.**
6. **English version is authentic.**

Q.1 Answer any seven out of ten. **14**

1. The output of an AND gate with three inputs, A, B, and C, is HIGH when _____.
   A. A = 1, B = 1, C = 0 B. A = 1, B = 1, C = 1
   C. A = 0, B = 0, C = 0 D. A = 1, B = 0, C = 1
2. What is the octal equivalent of the binary number (10111101)2.
   A. 675 B. 275
   C. 572 D. 573
3. A NAND gate is called a universal logic element because
   A. it is used by everybody
   B. any logic function can be realized by NAND gates alone
   C. Many digital computers use NAND gates.
   D. all the minization techniques are applicable for optimum NAND gate realization
4. Positive logic in a logic circuit is one in which
   A. logic 0 and 1 are represented by 0 and positive voltage respectively
   B. logic 0 and, -1 are represented by negative and positive voltages respectively
   C. logic 0 voltage level is higher than logic 1 voltage level
   D. logic 0 voltage level is lower than logic 1 voltage level.
5. Half Adder circuit is
   A. Half of an AND gate B.A circuit to add two bits together
   C. Half of a NAND gate D. None of these
6. The basic storage element in a digital system is
   A. Flip flop B. Counter
   C. Multiplexer D. Encoder
7. In a shift-right register, shifting a bit by one bit means
   A. Division by 2 B. Subtraction by 2
   C. Multiplication by 2 D. None of these
8. Which of the following is correct?
   A. A.A'=A B. A+A'=A'
   C. A.A'=0 D. A+A'=A
9. How many flip-flops are required to construct a Mod-10 counter?
   A. 10 B. 8
   C. 5 D. 4
10. AB + AB' =
    A. A B. B'

C. A' D. B

Q.2	(a)	Perform subtraction using 1's-complement method $(100110)_2$ - $(110010)_2$	**03**
		OR	
	(a)	Simplify Y = AB'C + AB using Boolean algebra.	**03**
	(b)	Perform subtraction using 2's-complement method $(110101)_2$ - $(110010)_2$	**03**
		OR	
	(b)	Multiply the following binary number: $(101111)_2$ X $(101)_2$	**03**
	(c)	Two 4-bit binary numbers (1001 and 1101) are applied to a 4-bit parallel adder. What are the values for the sum and carry output?	**04**
		OR	
	(c)	Implement OR and AND gates using NOR gates.	**04**
	(d)	Explain Half Adder circuit with the help of truth table.	**04**
		OR	
	(d)	What are the differences between combinational logic and sequential logic?	**04**
Q.3	(a)	Explain Half Subtractor circuit with the help of truth table.	**03**
		OR	
	(a)	Draw circuit diagram of 4-bit UP/DOWN Counter.	**03**
	(b)	Implement Binary to Gray Code Converter using Ex-OR gates.	**03**
		OR	
	(b)	How can you convert the JK Flip-flop into Toggle Flip-flop?	**03**
	(c)	Obtain SOP simplification form of following expression using Karnaugh map $F(A,B,C,D)=\Sigma m(1, 2, 3, 5, 6, 7, 9, 13, 15)$	**04**
		OR	
	(c)	State De-morgan's theorems and write their expressions.	**04**
	(d)	Draw any logic components for pressure loop for pressure switch configuration HL.	**04**
		OR	
	(d)	Explain working of level loop for level switch configuration HL.	**04**
Q.4	(a)	Draw any logic components for level loop for level switch configuration LL.	**03**
		OR	
	(a)	List applications of D/A Convertor in instrumentation.	**03**
	(b)	Implement Full Adder circuit.	**04**
		OR	
	(b)	Implement Odd-Parity Generator circuit.	**04**
	(c)	What is a multiplexer? Implement 4:1 line multiplexer with truth-table.	**07**
Q.5	(a)	Implement Full Subtractor circuit.	**04**
	(b)	Draw any logic components for level loop for level switch configuration HL.	**04**
	(c)	Draw a circuit diagram of 3 X 8 line Decoder	**03**
	(d)	Simplify AB'C + ABC+ A'BC+ ABC'+ A'B'C and draw its logic diagram with minimum gates.	**03**